UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,734	03/30/2000	Per Hammarlund	042390.P6873	8889

7590 11/26/2004

Andre l Marais
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/539,734	HAMMARLUND ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-14,16,18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4, 6-14, 16, 18, and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2, 4, 6-11, 13-14, 16, 18, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrofer U.S. Patent Number 4,682,284 (herein referred to as Schrofer) in view of Joshi et al, U.S. Patent Number 5,954,815 (herein referred to as Joshi) in further in view of Mitchell et al, U.S. Patent Number 4,841,476 (herein referred to as Mitchell).

2. Referring to claims 1 and 21 Schrofer has taught a method including:

in a queue, writing a first object of a plurality of objects to a first location indicated by a write pointer (Schrofer column 3 lines 10-15);

making a qualitative determination whether or not to retain the first object within the queue based on the indicated invalidity of the first object (Schrofer column 3 lines 13-32);

if the qualitative determination is to retain the first object, then advancing the write pointer to indicate a second location within the queue into which to write a second object (Schrofer column 3 lines 10-32); and

if the qualitative determination is not to retain the first object, then maintaining the write pointer to indicate the first location within the queue into which to write the second object, so that the first object is overwritten by the second object (Schrofer column 3 lines 10-32). Schrofer has not explicitly taught where the object stored in the first location was a microinstruction. Schrofer has also not taught the plurality of instructions being written to the queue as a set of predetermined number of instructions, and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions.

3. Joshi has taught where the object stored in the first location was an instruction and where there is a plurality of instructions (Joshi abstract, figure 3, column 4 lines 12-15). Joshi has also taught the plurality of instructions being written to the queue as a set of predetermined number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions (Joshi column 7 lines 1-21; where the instructions that are after the delay instruction are indicated as being invalid, since they are outside of a trace of instructions; therefore if the first instruction comes after a delay instruction, it would be outside a specified trace, since it comes after a specified point, and then is considered to be invalid). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi. Both teach storing information into entries of a queue. One of ordinary skill in the art at the time of the invention would recognize that instructions could be stored in the queue of Schrofer after the

instructions have been fetched from an instruction cache (Joshi figure 3 reference number 50 column 4 lines 1-11). By fetching the maximum number of instructions before they are needed every time, which would make the number predetermined, and storing them in a queue allows the processor to have quick access to the instructions when it is ready to decode and/or execute the instructions. Now, when the processor is ready for the instructions, they are waiting in a queue in the processor and do not have to be fetched from some other memory, which delays the execution of that instruction. This is known as prefetching, and was a common method in the art at the time of the invention. Also, if the system does not want to execute certain instructions, for example if they follow a wrong branch prediction, then those instructions should be invalidated as taught in Joshi, so that the system does not waste clock cycles and time performing these operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi to reduce the access time needed to fetch instructions since the instructions are ready and waiting in a queue.

4. The combination of Schrofer and Joshi has not taught wherein the first instruction comprises a first microinstruction. Mitchell has taught wherein the first instruction comprises a first microinstruction (Mitchell figure 2, column 4 lines 35-39). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Mitchell. Microinstructions are used in many modern computers today, such as RISC systems. By definition, microinstructions are derived from a macroinstruction. Therefore, any microinstructions would come from a macroinstructions and then decoded, or emulated, into smaller operations or microinstructions. Microinstructions need to be stored in queues before, after, and/or during execution, just as any

other instruction is stored so that the instructions are easily accessible with quick access time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Mitchell so that the microinstructions can be accessed by various parts of the processor from queues with small access times, which reduce the time for execution.

5. Referring to claim 13 Schrofer has taught an apparatus comprising:

a queue to buffer a first object propagated from a source to a destination (Schrofer column 3 lines 10-15); and

write logic to make a qualitative determination whether or not to retain the first object within the queue (Schrofer column 3 lines 13-16); if the qualitative determination is to retain the first instruction, to advance a write pointer to indicate a second location within the queue into which to write a second object; and, if the qualitative determination is not to retain the first object, to maintain the write pointer to indicate the first location within the queue into which to write the second object, so that the first object is overwritten by the second object (Schrofer column 3 lines 10-32).

Schrofer has not explicitly taught where the object stored in the first location was an instruction. Schrofer has also not taught the plurality of instructions being written to the queue as a set of predetermined number of instructions, and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions.

Joshi has taught where the object stored in the first location was an instruction and where there is a plurality of instructions (Joshi abstract, figure 3, column 4 lines 12-15). Joshi has also taught the plurality of instructions being written to the queue as a set of predetermined number of

instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions (Joshi column 7 lines 1-21; where the instructions that are after the delay instruction are indicated as being invalid, since they are outside of a trace of instructions; therefore if the first instruction comes after a delay instruction, it would be outside a specified trace, since it comes after a specified point, and then is considered to be invalid). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi. Both teach storing information into entries of a queue. One of ordinary skill in the art at the time of the invention would recognize that instructions could be stored in the queue of Schrofer after the instructions have been fetched from an instruction cache (Joshi figure 3 reference number 50 column 4 lines 1-11). By fetching the maximum number of instructions before they are needed every time, which would make the number predetermined, and storing them in a queue allows the processor to have quick access to the instructions when it is ready to decode and/or execute the instructions. Now, when the processor is ready for the instructions, they are waiting in a queue in the processor and do not have to be fetched from some other memory, which delays the execution of that instruction. This is known as prefetching, and was a common method in the art at the time of the invention. Also, if the system does not want to execute certain instructions, for example if they follow a wrong branch prediction, then those instructions should be invalidated as taught in Joshi, so that the system does not waste clock cycles and time performing these

operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi to reduce the access time needed to fetch instructions since the instructions are ready and waiting in a queue.

6. Referring to claims 2 and 14 Schrofer has taught wherein the qualitative determination includes examining a valid bit associated with the first instruction to determine validity of the first instruction (Schrofer figure 4 reference numbers 310,315, and 301 column 11 lines 16-25), making the qualitative determination to retain the first instruction if the valid bit indicates the first instruction is being valid, and making the qualitative determination not to retain the first instruction if the valid bit indicates the first instruction as being invalid (Schrofer column 3 lines 10-32).

7. Referring to claims 4 and 16 the combination of Schrofer and Joshi has taught wherein a plurality of instructions are written to the queue in a set of a predetermined number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and wherein at least one instruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch instruction upstream of the at least one instruction in a stream of instructions (Joshi column 6 lines 35-53 and column 7 lines 1-21).

8. Referring to claim 9 the combination of Schrofer and Joshi has taught wherein the first instruction is received into the queue as part of a set of instructions comprising a first predetermined number of instructions and read from the queue to an instruction destination as

part of a second set of instructions comprising a second number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, and since different instructions are dispatched to different execution paths, shown in figure 3 reference numbers 74 and 82, instructions in some paths will take longer or shorter amounts of times, depending on the path it is in, therefore being part of different sets of instructions when it enters the queue and when it leaves the queue).

9. Referring to claims 10 and 20 Schrofer has taught wherein the first instruction is written from a source to a destination, and wherein the queue comprises a first path between source and destination, the method including propagating the first instruction from the source to the destination via a second path, not including the queue, if the queue is empty (Schrofer column 3 lines 40-58).

10. Referring to claim 11 Schrofer has taught including selecting between the first and second paths to receive the first instruction for propagation to the destination (Schrofer column 3 lines 40-58).

11. Referring to claim 22 Schrofer has taught wherein the sequence of instructions cause a multiprocessor to perform the step of examining a valid bit associated with the instruction to determine validity of the first instruction (Schrofer figure 4 reference numbers 310,315, and 301 column 11 lines 16-25), to make the qualitative determination to retain the first instruction if the valid bit indicates the first instruction as being valid, and to make the qualitative determination

not to retain the first instruction if the valid bit indicates the first instruction as being invalid (Schrofer column 3 lines 10-32)..

12. Referring to claims 6 and 18 the combination of Schrofer, Joshi, and Mitchell has taught wherein the first microinstruction is written to the queue from a microinstruction cache (Mitchell figure 2, column 4 lines 35-39).

13. Referring to claim 7 the combination of Schrofer, Joshi, and Mitchell has taught wherein the first microinstruction is part of a trace of microinstructions received from the microinstruction cache (Joshi column 4 lines 7-11 and line 51-column 5 line16; Joshi teaches that several instructions are dispatched from the cache to the queue, as part of a trace).

14. Referring to claim 8 the combination of Schrofer, Joshi, Panwar, and Mitchell has taught wherein the first instruction is received from an instruction source operating in a first clocking domain into the queue and read from the queue to an instruction destination operating in a second clocking domain (Schrofer column 9 line 62-column 10 line 15; it is described here where the clock signal that writes information into the queue is at a different frequency than the clock signal that is used to read information out of the queue).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Schrofer and Joshi and Mitchell in view of Nemirovsky et al, U.S. Patent Number 6,477,562 (herein referred to as Nemirovsky).

16. Referring to claim 12 the combination of Schrofer and Joshi has not taught wherein the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which the first instruction is written is located in the first portion if the first

instruction comprises part of the first thread. Nemirovsky has taught wherein the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which the first instruction is written is located in the first portion if the first instruction comprises part of the first thread (Nemirovsky column 6 line 65-column 7 line 11; since a single queue could be partitioned for separate threads, it would be inherent that if one partition was allocated for a particular thread, than an instruction pertaining to that thread would be placed in that partition, or portion). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Nemirovsky so that the queue would be partitioned for multithreaded processing. By having separate portions or partitions in the queue for different threads allows the scheduler that dedicates different resources to the individual threads to easily access the instructions from the individual threads. When the scheduler is to send an instruction from thread 2, for example, it may go to the first entry from the second portion of the queue to find the next instruction for that thread, instead of searching through all the instructions for the next instruction for the second thread, which would result in a longer delay. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have separate portions or partitions in the queue for individual threads to reduce the amount of time to find and access the next instruction to be processed from a particular thread.

Response to Arguments

17. Applicant's arguments filed 08/24/04 have been fully considered but they are not persuasive.

18. In the remarks, in regard to the rejections of claims, Applicant argues in essence that:

"Although Mitchell discloses an instruction cache, which contains microinstructions (Mitchell, 4: 35-39), Mitchell fails to disclose or even suggest 'the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions, the trace of microinstructions corresponding to a macroinstruction and comprising a sequence of microinstructions', as required by claim 1.

Thus, the Applicants submit that a combination of Mitchell and Joshi does not yield the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions", as required by claim 1. Thus, claim 1 and its dependent claims 2, 4, and 6-12 are patentable over Schrofer, whether considered separately or in combination with Joshi and Mitchell, and should be allowed."

19. This is not found persuasive. As the Applicant points out, the Office Action shows where Joshi has taught "the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions" (Joshi column 7 lines 1-21), as shown in paragraph 3, in the rejections above. Mitchell is relied upon to teach the idea of microinstructions. One of ordinary skill in the art at the time of the invention would recognize that using microinstructions is well known in the art, and that a sequence of microinstructions correspond to macroinstructions. The Modern Dictionary of Electronics, copyright dated in 1988, is being submitted as extrinsic evidence, and teach that a microinstruction sequence is known to be from the microprogram that executes a macroinstruction. In addition, Mitchell is not called on to teach "the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions", but to teach the concept of microinstructions and sequences of microinstructions, which as shown by the Modern Dictionary of Electronics, comes from macroinstructions.

20. Applicant is also reminded that, in response to arguments against the references individually, one cannot show nonobviousness by attacking references individually where the

rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness
Examiner
Art Unit 2183
November 19, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100